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CONTACT

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ADMINISTRATIVE SECRETARIAT

MBTechnoServices | essxrc2022@MBTechnoServices.com

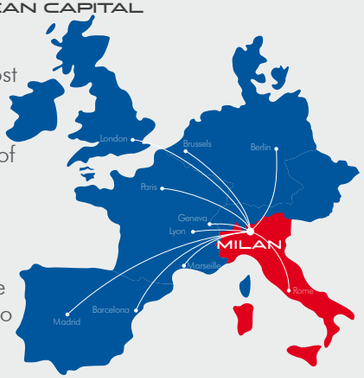
SSCS IEEE Electron Devices Society

INTELLIGENT ELECTRONICS

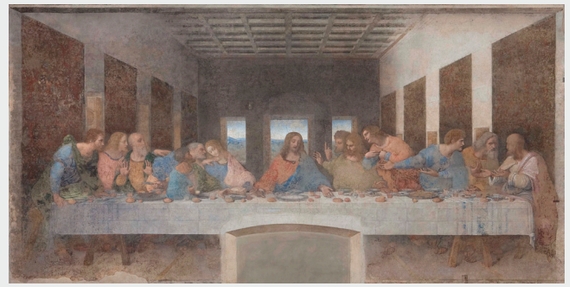
for a smarter and more inclusive Human Life

WWW.ESSCIRC-ESSDERC2022.ORG

MILAN - A EUROPEAN CAPITAL



Founded in 590 B.C., Milan is one of the most important Italian and European cities.
It is the Italian capital of finance (with the Stock Exchange site – La Borsa), of fashion and of design.
Milan is an Art city: the iconic Duomo, Castello Sforzesco, and Santa Maria delle Grazie with Leonardo's 'Last supper' are only few of the several monuments to be visited in the city, where Leonardo da Vinci lived and left significant demonstration of his genius as collected and exhibited at the Technology National Museum Leonardo Da Vinci.



*by concession of Ministero della Cultura - Direzione Regionale Musei Lombardia

Milan is the most important Italian city from the industrial and technological point of view, as for the number of high and medium-high technology companies. An "Italian Silicon Valley" with 6,160 companies operating in the high (1,500) and medium-high technology sectors for a total of 140 thousand employees. These strategic companies in the Italian economic system represent 26% of the number of companies in the Milan area, almost twice the national figure (14%).

VENUE

The venue of the conference events, including workshops and tutorials, will be at the University of Milan-Bicocca (Milan, IT), that is well connected (metro, bus, train with Milan downtown).

GENERAL PURPOSE OF THE CONFERENCE

The aim of **ESSCIRC** and **ESSDERC** is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on- chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary.
While keeping separate Technical Program Committees, **ESSCIRC** and **ESSDERC** are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

CONFERENCE TRACKS

Although not limited, papers are solicited for the following main topics:

- **Advanced Technology, Process and Materials** Process and material developments for logic, memory, and non-CMOS, including electrical and physico-chemical characterization, process integration and manufacturing: 2D TMDs and related insulators (e.g., hBN), graphene, TFTs, gate oxide, gate material, silicide, MOL and BEOL materials, 3D monolithic as well as conventional and novel memory cells including charge-based memories, ReRAM, MRAM, PCRAM, ferroelectrics, crosspoint and selectors, organic memory.

- **Analog, Power and RF Devices** From material growth to device, components, and systems (process, design, devices fabrication, applications). Device design and electrical/physical/electro-thermal/reliability characterization of devices based on Si RF CMOS, RF SOI, SiGe HBTs, SiC, InP/InGaAs/GaAs, AlGaN/InGaN/GaN, CNT, diamond and related material systems. Power systems integration issues including thermal management, packaging technologies, system-level electro thermal characterization, product quality and system reliability aspects. Device production processes and design for manufacturability.

- **Compact modeling and process/device simulation** TCAD and advanced simulation techniques and studies, compact/SPICE modeling of electronic, optical, organic, emerging, and hybrid devices and their IC implementation and interconnection. Verilog-A models of semiconductor devices (including bio/med sensors, MEMS, microwave, RF, high voltage and power, emerging technologies, and novel devices), parameter extraction, reliability and variability, performance evaluation and open-source benchmarking/implementation methodologies. Modeling of interactions between process, device and circuit design, design/technology co-optimization, foundry/fabless interface strategies. Numerical, analytical, statistical modeling and simulation of electronic, optical and hybrid devices, interconnect, isolation, and 2D/3D integration. Simulations of material properties and fabrication processes. Advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport). Mechanical and/or electro-thermal modeling and simulation. Simulations of reliability aspects of materials and devices.

- **Analog** Amplifiers, drivers, comparators, filters, references, analog systems, and analog techniques.

- **Data Converters** Nyquist-rate and oversampling A/D and D/A converters. Capacitance-to-digital, time-to-digital, frequency-to-digital converters. Embedded and application-specific A/D and D/A converters. Analog to information conversion. A/D and D/A converter building blocks (sample-and-hold circuits, calibration circuits). Enabling new techniques, architectures, or technologies.

- **RF & mm-Wave** Building blocks operating at RF, mm-Wave and THz frequencies for wireless communication, radar, sensing, and imaging.

- **Frequency Generation Circuits** Oscillators and controlled oscillators, PLL, DLL, injection locked oscillators, frequency dividers, any kind of frequency generation or time base circuits and systems.

- **Digital Circuits & Systems** Digital circuits and memory subsystems for microprocessors, micro-controllers, application processors, graphics processors; digital systems for communications, video, and multimedia. Digital design techniques for power reduction, intra-chip communication, clock distribution, soft-error and variation-tolerant design, system-level integration.

- **Power Management** Power management and control circuits. Regulators. Switched-mode power converter ICs using inductive, capacitive, and hybrid techniques. Energy harvesting circuits and systems. Wide-bandgap topologies and gate-drivers. Power and signal isolators; robust power management circuits for automotive and other harsh environments. Circuits for lighting, wireless power and envelope modulators. Design for manufacturability

- **Wireless & Wireline Circuits & Systems** Wireless and wireline circuits and systems, 2.5/3D interconnect, copper-cable links, and equalizing on-chip links, exploratory I/O circuits for advancing data rates, radio transceiver SoC or SiP at RF/mmW and THz frequencies, chip to chip system communications, high speed serial interfaces, optical interfaces, established standards communication system full chip solutions.

- **Emerging Computing Devices and Circuits** Advanced CMOS, post-CMOS, quantum computing, cryogenic circuits, novel device and circuit concepts that improve existing and enable novel computing paradigms. Advanced CMOS and beyond CMOS transistors (tunnel FET, negative capacitance FET), transistors based on low-dimensional systems (2D materials, nanowires, and quantum dots), and on topological insulators, as well as phase transitions transistors and all kind of circuit implementations with such devices. Qubit devices for quantum computing enabling and all related cryogenic circuits. Non-charge-based logic devices and circuits (magnetic logic, spintronics, and plasmonics).

- **Memory Devices & Circuits Towards Non-von Neumann** Neuromorphic computing, AI accelerators, in-memory-computing, security. Emerging devices and materials in neuromorphic computing. New materials, and new uses for established materials, within the context of neuromorphic computing algorithms, ranging from deep neural networks (deep learning) to more bio-inspired networks and algorithms. Resistive switching materials, including phase change and ferroelectric materials for neuromorphic computing, materials for spintronic implementations of neuromorphic computing. Edge and cloud AI computing platforms. Silicon implementation of neuromorphic circuits, processors, systems and their applications. In-memory-computing and logic-in-memory. Phenomena, devices, circuits, and systems for IoT and IoE security (e.g., PUFs, TRNGs).

- **Devices & Circuits for Sensors, Optoelectronics & Display** Devices and circuits based on MEMS and bioelectronics devices for biomedical and imaging applications. Image sensors and related circuits and systems, SoCs. Automotive, LIDAR, and ultrasonic sensors for ADAS, autonomous driving, smart mobility. MEMS sensor systems. Wearable, implantable, ingestible electronics, biomedical SoCs, neural interfaces and closed-loop systems. Biosensors, microarrays, and lab-on-a-chip. Display electronics, displays with sensing functionality. Devices, circuits, and systems for AR/VR and related sensing/actuation. Product quality and reliability aspects. Device and circuits production processes and design for manufacturability

CONFERENCE HIGHLIGHTS

- 4 joint keynote presentations
- 3 **ESSDERC** keynote presentations
- 3 **ESSCIRC** keynote presentations
- Invited papers with overall coverage of all aspects of advanced devices and circuits
- Presentation of IEEE and **ESSCIRC**/**ESSDERC** Awards
- **ESSCIRC**/**ESSDERC** Welcome Reception on Tuesday, September 20, 2022
- **ESSCIRC**/**ESSDERC** Gala Dinner on Wednesday, September 21, 2022
- Several Workshops and Tutorials about the most interesting topics in the microelectronics field will be offered on September 19, 2022. Participants in Workshops and Tutorials will have the opportunity to give an on-line final exam for ECTS acquisition.

The working language of the conference is English.

PAPER SUBMISSION

Manuscript guidelines as well as instructions on how to submit electronically will be available on the conference website.
Papers must not exceed four A4 pages with all illustrations and references included.

THE PAPERS SUBMISSION DEADLINE: APRIL 12, 2022

Papers submitted for review must clearly state:

- The purpose of the work
- How and to what extent it advances the state-of-the art
- Specific results and their impact

Only work that has not been previously published or submitted elsewhere will be considered. Submission of a paper for review and subsequent acceptance is considered as a commitment that the work will not be publicly available prior to the conference.

After selection of papers, the authors will be informed about the decision of the Technical Program Committee by e-mail by 31 May 2022.

At the same time, the complete program will be published on the conference website. A binary feedback (accepted/rejected) with no comments will be provided to the authors. An oral presentation will be given at the Conference for each accepted paper. No-shows will result in the exclusion of the papers from any conference related publication.
The submitted final PDF files should be IEEE Xplore compliant.

For each paper independently, at least one (co-)author is required to register for the Conference before 31 July 2022 (one registration-one paper policy).
Registration fees will be available on the conference website.