

IEEE 31st INTERNATIONAL SYMPOSIUM ON THE PHYSICAL AND FAILURE ANALYSIS OF INTEGRATED CIRCUITS (IPFA)

July 15 – 18, 2024

Sands Expo and Convention Centre,
SINGAPORE

1st CALL FOR PAPERS

IPFA is devoted to the fundamental understanding of the electrical and physical characterization techniques and associated technologies that assist in probing the nature of failures in conventional, modern and new Semiconductor devices. The Technical Program Committee is inviting papers related, but not limited to, the following areas:

FAILURE ANALYSIS (FA) TRACKS

RELIABILITY (REL) TRACKS

FA1: Sample Preparation, Metrology and Defect Characterization:

Device de-processing, Ion beam / TEM sample preparation, Metrology, Defect inspection, Test chips.

FA2: Electrical Fault Isolation Techniques: Photon, Laser and Electron beam-based microscopy techniques, Static and Tester based techniques, Nanoprobing, AFP, EBAC/EBIC, Next-generation backside power-rail analysis.

FA3: Case Studies on Fault Isolation: Application of non-destructive workflows for defect localization. Die / Board / System-level electrical FA, Electrical characterization and nanoprobing.

FA4: Physical Failure Analysis Techniques: Advanced methodologies in PFA, Advanced optical/Ion beam approaches, Plasma/Laser FIB, Spectroscopy (EDX/EELS/SIMS) techniques, Scanning probe microscopy, Circuit-edits, De-layering recipe innovations, Tomography.

FA5: Case Studies on Physical Failure Analysis: Die / Board / System-level physical FA, Workflows, Defect exposure and characterization in silicon devices.

FA6: Board, System and Product Level Failure Analysis: Design for manufacturing, Test diagnostics, Volume and statistical analysis, Construction Analysis, Reverse engineering. Embedded BIST and DFT test and diagnosis, reliability testing, defect-oriented testing, protocol-aware testing, Test-to-Design feedback, mixed signal and analog tests, silicon failure debug by test and yield engineering methodologies, yield analysis and optimization

FA7: Package-Level Failure Analysis Techniques: Heterogenous integration, 2.5D/3D/SiP Package FA, backside power delivery network, Non-destructive analysis including Magnetic/acoustic/ X-ray/ Lock-in thermography/ FTIR, TDR, EOTPR, material analysis

FA8: Case Studies on Package-Level Failure Analysis: Workflows in Packaging FA, defect localization, exposure & characterization in packaging. Flip-chips, Wire-bond, 2.5D/3D/SiP, wafer & panel analysis

REL1: Transistor and Emerging Electron Devices Reliability: Gate oxide/High-k reliability, PBTI/NBTI, dopant effects, Self Heating in CMOS, GAA FET / RFSOI/ HBM / stack DRAM device reliability, Process and stress-induced reliability issues and variability, Non-volatile memory reliability – retention, endurance and read disturb in PCRAM, RRAM, STT-MRAM, Reliability and characterization of ferroelectric devices.

REL2: Interconnect and Packaging Reliability: modeling and simulation TDDB dielectrics, Electro and stress migration, cracking, corrosion, and fatigue in bond pads, Reliability of 3DIC/ TSV, Heterogeneous Integration in SiP, Thermo-mechanical stress, Power, Wafer warpage, Wire and wafer bonding, chip-package interaction

REL3: ESD, Latchup, Reliability for Space and Nuclear Radiation: Component and system level ESD design: modeling and simulation, Neutron and alpha particle single event radiation, SER/SEU

SPECIALIZED TECHNOLOGY (ST) TRACKS

ST1: Hardware Security: Semi-Invasive and Invasive Analysis for attack of encryption system and countermeasure, Die-Level Reverse Engineering, Counterfeit Electronics Detection, Hardware Trojan localization

ST2: AI for Failure Analysis and Reliability: Artificial intelligence (AI) for FA – fault detection, visual / image analytics, pattern recognition, signal processing, Machine learning for prognosis & reliability. Reliability assessment for new applications (e.g. neuromorphic devices and AI accelerators).

ST3: High Power Electronics / Wide Bandgap Device Reliability & Failure Analysis: Reliability and FA of GaAs, GaN, SiC and Ga₂O₃ devices, Trap-related degradation, Materials-related defect characterization, Process variability, III-V/Si integration and case studies of defects.

ST4: Optoelectronics & MEMS Device Reliability & Failure Analysis: Reliability and FA on display modules, lasers, LEDs, solar cells (silicon, CdTe, CIGS, organic materials, multi-junction, perovskite), CMOS image sensors, Photodetectors, Waveguides, Silicon Photonics, MEMS devices, flexible electronics and thermoelectrics.

NORMAL MODE SUBMISSION

- ❖ Extended Abstract Submission: 21 Jan 24
- ❖ Notification of Acceptance: 18 Mar 24
- ❖ Full Manuscript Submission: 22 Apr 24
- ❖ Final Manuscript Submission: 01 Jun 24

EXPRESS MODE SUBMISSION



- ❖ Direct Full Paper Submission: 21 Jan 24
- ❖ Notification of Acceptance: 18 Mar 24
- ❖ Final Manuscript Submission: 01 Jun 24

- **NORMAL Mode Submission** - Extended abstract (min. **2 pages**, incl. text and figures) of your original research work. Accepted abstracts will require a full manuscript (min 4 pages) to be submitted by 22nd Apr and post-mentored final manuscripts by 1st Jun.
- **EXPRESS Mode Submission** - Full Manuscript (Min. **4 pages**, incl. texts and figures) that is a complete write-up of your original research. This allows you to skip one submission setup and more time for legal approval of your post-mentored final manuscript.
- Details on abstract / manuscript submission, templates and other information are available at <https://www.ipfa-ieee.org/2024>
- Authors of high quality papers presented at IPFA 2024 will be invited to submit an **extended version** of their work for a Special Issue in *Elsevier Journal - Microelectronic Engineering*, (IF: 2.3). Expected publication in Feb-Mar 2025.

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