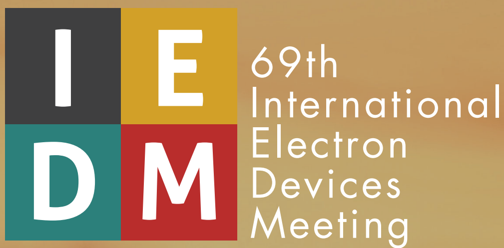


2023 IEDM Conference Theme

Devices for a Smart World Built Upon 60 Years of CMOS

For More Information

IEDM Online: ieee-iedm.org

Social Networks:
ieee-iedm.org/social-media

2023 IEEE International Electron Devices Meeting

December 9-13, 2023

Hilton San Francisco Union Square
San Francisco, California

Call for Papers

Submission deadline: July 13th

Single submission of final, four-page paper

Topics

IEDM encourages submissions in all areas with special emphasis on:

- Neuromorphic / compute in memory / AI
- Quantum computing devices
- Devices for RF, 5G/6G, THz and mm-wave
- Advanced memory technologies
- Advanced logic technologies and power distribution network
- Novel materials for next generation devices
- Non-charge-based materials, devices and systems
- Advanced power devices, modules and systems
- Sensors, MEMS and bioelectronics
- Devices/circuits/system interaction
- Advanced Packaging, and package-device level interactions
- Electron device simulation and modeling
- Reliability of systems and electronic devices
- Robustness/security of electronic circuits and systems
- Optoelectronics, displays and imaging systems

Meeting Highlights

- Three plenary presentations by prominent experts
- Special focus sessions covering topics in:
  - Sustainability in Semiconductor Device Technology and Manufacturing
  - Logic, Memory, Package and System Technologies for Future Generative AI
  - 3D Stacking for Next-Generation Logic & Memory by Wafer Bonding and Related Technologies
  - Neuromorphic Computing for Smart Sensors
- Evening Panel Discussions
- Six tutorial sessions on Saturday, December 9th
- Two short courses on Sunday, December 10th
- Exhibits on December 11th – 13th

Papers in the Following Areas Are Requested

ADVANCED LOGIC TECHNOLOGY (ALT): Papers are solicited in the areas of CMOS platform technologies and applications (e.g., HPC, LOP, mobile, automotive, low-temperature CMOS, etc.), logic devices and circuits, process integration schemes for advanced nodes, innovations in material, process and metrology techniques, and design technology co-optimization (DTCO) and system technology co-optimization (STCO). Platform technologies include state-of-the-art Si and beyond-Si channel devices, gate-all-around devices, stacked devices with different polarity transistors, advanced interconnect, novel power distribution integration schemes, heterogenous 2.5D/3D integration schemes, and BEOL compatible transistors. Device architecture, device design and analysis, process integration, module advancements in process and patterning, metrology, physical layout effects, techniques for reduced variability, yield, thermal management, methodologies and solutions for DTCO/STCO in the solicited areas are of high interest.

EMERGING DEVICE and COMPUTE TECHNOLOGY (EDT): Papers are solicited on emerging nano-electronic devices and physics. This includes devices based on novel transport and control mechanisms such as tunnel FET, negative capacitance FET, cold-source FET, topological materials and devices, phase transitions, ferroelectrics and quantum effects. Devices based on low-dimensional systems including 2D materials, CNTs, nanowires, single electron transistors and quantum dots are welcomed. Exploratory devices with novel device functions and/or novel materials for neuromorphic compute, approximate and analog compute, and non-charge-based compute such as spintronics are key topics. Furthermore, emerging state machines and time dynamical compute systems are also of interest. Qubit devices as well as devices and systems designed to enable quantum computing, quantum simulation and quantum annealing are of high interest. Papers in EDT focus primarily on device physics and novel elaboration concepts.

MEMORY TECHNOLOGY (MT): Papers are solicited in the areas related to embedded and standalone memory technology. This includes advances in both conventional memories including SRAM, DRAM and Flash, and emerging memories including ReRAM, MRAM, PCRAM, ferroelectric memory, crosspoint memory and selectors, organic memory and NEMS-based memory, as well as their applications in the areas of AI and near-Memory compute. Topics span from demonstration of novel device concepts to fully integrated memory arrays, and from product prototyping to manufacturing related challenges and solutions. Demonstrations of manufacturing maturity of emerging memories and future scaling of conventional memories to solve the memory wall issues are of high interest. Submission of papers on novel device concepts and demonstrations, novel integration schemes, novel circuit design schemes, and novel memory architectures that enhance memory performance, scaling, 3D stacking, capacity/bandwidth increasing, and power/energy reduction are strongly encouraged. Papers based on novel device physics and in-memory computing may be transferred to EDT or NC at the discretion of the committee.

POWER, MILLIMETER WAVE and ANALOG TECHNOLOGY (PMA): Contributions are sought on novel circuit topologies, manufacturing processes, supporting modeling (TCAD and compact models), device physics, reliability, and materials (SiC, (Al)GaN, diamond, Ga2O3, Si, III-Vs, etc.) along with fundamental studies on doping, deep-level traps, interface state densities, and device reliability for power and/or high frequency devices. Papers are solicited on discrete and integrated power and/or high frequency (micro, mm-wave and THz) devices and physics, modules and systems. Topics of interest include devices (diodes, BJTs, FETs, super-junction devices, heterostructures, IGBTs, HEMTs, HBTs, light-triggered structures for galvanic isolation and faster switching, bi-directional switches, vertical geometry devices, etc.) and device/package/circuit interactions, including thermal management. Wide variety of applications are also of interest (power conversion, supply, regulation and conditioning for computers and data centers, motor drives, transportation, solar, wind, smart grid applications, wireless power harvesting/transfer, filters, beam formers, power amplifiers, tunable passives, antenna arrays, SAW/BAW).

MODELING and SIMULATION (MS): Papers are solicited on theoretical approaches to electronic devices, including logic devices, memory devices, optical devices, interconnects and (bio)sensors. Theoretical approaches include analytical, numerical, statistical, and machine-learning/AI-based approaches applied to structures with dimensions ranging from atomistic over device dimensions to full-chip dimensions, including physics-based compact modeling. Key to submissions is, that the device innovation is central, either through predictive insight in the potential of novel device concepts, predictive analysis revealing significant improvement to devices, breakthroughs in the theoretical understanding of the device operation, breakthroughs in the understanding of device processing enabling improved device performance, novel insights in variability, reliability and yield issues, breakthrough in device optimization based on DTCO. Topics also include ab-initio/atomistic materials modeling, modeling of neuromorphic computing, quantum computing, spintronics, low-dimensional devices, ferroelectrics, thermal modeling, 3D/heterogeneous integration, electro-chemical/mechanical devices. Comparison with experimental data, model calibration and multi-scale simulation chains are highly encouraged.

OPTOELECTRONICS, DISPLAYS, and IMAGING SYSTEMS (ODI): Papers are solicited on optoelectronics, displays, and imaging systems. This includes novel devices, structures, and integration for image sensors, displays, light sources, photonic devices, and high-speed photodetectors and modulators. New technologies on heterogeneous integration of optoelectronics as well as on photonic-electronic integration for optical interconnects, on-chip networks and sensing are welcomed. Papers on quantum photonics, neuromorphic photonics, and plasmonics for quantum computation, sensing and encryption are also of interest. Furthermore, ODI includes CMOS imagers, high-speed and high-time resolution imagers, CCDs, stacked, single-photon and non-visible image sensors. In addition, papers on displays for augmented or virtual reality, holography, TFTs for photonics applications, flexible, stretchable, and/or printed electronics, in-display sensors are encouraged. Papers on displays or light emitting devices with novel materials such as perovskites or quantum dots are also of interest. We particularly welcome submissions concerning optoelectronic or photonic devices or systems based on topological concepts.

NEUROMORPHIC COMPUTING (NC): Papers are solicited in the areas related to devices, circuits, and algorithms for neuromorphic computing and AI. We welcome submissions covering a wide range of areas in neuromorphic computing including but not limited to: analog in-memory deep learning, compute-in-memory, probabilistic/approximate/analog computing, combinatorial optimization, machine learning, and AI applications, edge computing, unclonable functions, reservoir computing, spiking neural network, artificial intelligence, in-sensor computing, and bio-inspired computing based on memory/logic/sensor/nanoelectronic/MEMS devices and their novel architecture and physics. Demonstration of real-world applications, full hardware integration, device-algorithm co-optimization, novel device concepts improving computational efficiency, and new algorithms mitigating non-ideal properties of devices and materials are of high interest.

RELIABILITY of SYSTEMS & DEVICES (RSD): Papers are solicited in reliability evaluation (experimental and modeling) of logic and memory devices, interconnects, and circuits and systems, mainly (but not limited) to employing Si-based technologies. Specific reliability topics include, for FEOL: transistor degradation due to hot carriers, bias temperature instabilities, random telegraph noise, and aging model; dielectric SILC and wear-out. For MEOL/BEOL, topics include breakdown of MEOL spacers and BEOL dielectrics; electromigration, stress migration failures of contacts and interconnects. For product, system, and circuit reliability, topics include latch-up, ESD, soft error mechanisms, variability-aware design, and design for reliability, robustness, and security of electronic circuits and systems. Of particular interest are investigations of degradation mechanisms for devices, circuits, and systems in the following areas: conventional and emerging memories; beyond CMOS devices; 3D IC package reliability, more-than-Moore applications; biomedical devices and systems; automotive and aerospace.

SENSORS, MEMS, and BIOELECTRONICS (SMB): Papers are solicited in the areas of sensors, micro/nano electromechanical systems (MEMS and NEMS), microfluidics/lab-on-chip, and BioMEMS, with particular emphasis on new device concepts, integrated and highly parallel CMOS implementations, CMOS-on-MEMS, embedded machine learning, organic-inorganic hybrid microfabrication, flexible devices, and multimodal sensors on a chip for applications in health, medicine, communication, mobility, and energy. Sensors include chemical, molecular and biological detection based on acoustic, electrical, electrochemical, magnetic, mechanical and optical principles. Topics of interest in the MEMS area include actuators, physical and biochemical sensors (BioMEMS), resonators, integrated inertial measurement units, RF MEMS, optomechanical devices, micro-power generators, and devices for energy harvesting as well as on-chip energy storage. Bioelectronics covers organic-inorganic hybrid devices, point-of-care biomedical devices, bio-electronic interfaces, integrated biomedical sensing, and implantable sensors and neural interfaces.

Preparation of Full Papers

Papers must be submitted electronically in IEEE Xplore-compatible pdf format. The deadline for submission of papers is July 13th, 2023. PRIOR to preparing your paper for electronic submission, please read the paper preparation and submission guidelines below. A paper template and sample paper are available at: ieee-iedm.org/preparation-of-papers

Papers Must Clearly State

- The purpose of the work
- The manner and degree to which it advances the art with proper references
- Specific new results that have been obtained with clear experimental (description of the work) conditions and their significance

The degree to which the paper deals with these issues will strongly affect whether the paper is accepted. The most common cause of rejection of submitted papers is a lack of specific results. Only those work that has not been previously published at the time of the conference will be considered. Paper acceptance will be based solely on the information provided on the four-page paper submitted. Promises of upcoming results will be ignored. All submissions will be checked for plagiarism.

Electronic Submission

Only electronic submissions through the paper submission system linked to the conference website will be accepted. Do not email files to the conference office. In order for your paper to receive a full review, the following information MUST be entered on the website along with your submission:

- Title of paper
- Name, complete mailing address and phone, and email of first author
- Names, affiliations, city, state, country of additional authors
- Person to whom correspondence should be sent, if other than the first author
- Identification as invited or student paper and student travel request, if applicable
- Suggested area (as listed in this announcement) into which the paper fits
- 50-word abstract

Papers Must Include

- Title of paper
- Name, complete mailing address, phone, and email of first author and name, affiliation, city, state and country of additional authors.
- 4 pages of two pages of text and two additional pages of figures and drawings (no text, captions only) in 8-1/2" x 11" format describing the planned 20-minute paper and emphasizing the findings. The font size for the body of the text and in figures and captions must be at least 10 point.
- Excessive photo reduction, poor legibility, and use of arbitrary units in figures may negatively impact acceptance.
- Papers with more than 2 pages of text or figures shall be grounds for immediate rejection.
- Please avoid the use of special international fonts.

50-Word Web Page Abstract

This abstract is a brief synopsis (50 words) of your paper. Accepted 50-word abstracts will be used in preparing the IEDM web pages. The abstract should be prepared and provided during the submission process in the requested text field on the submission web site. DO NOT INCLUDE the 50-word abstract as a separate page with your submission.

For questions contact the conference office:
iedm-info@ieee.org

Notification of Acceptance

Authors of accepted papers will be notified by the end of September. The accepted paper will be published as-is in the Technical Digest of the 2023 IEDM. Publication in the digest in no way precludes later publication of a fuller account of the work in another journal, but NO PUBLICATION is acceptable before the conference. The paper must be presented at the conference by one of the listed authors.

Student Presentation of Papers Encouraged

Papers presented by students and based on their own work will be considered for the Best Student Paper Award. The paper must be identified as a student paper at the time of submission. The award is based on both the paper and the presentation which must be given by the student. The award will be announced and presented at the 2024 IEDM.

Student Speaker Financial and Travel Assistance

Financial assistance for travel and registration is available to students presenting papers. This applies also for overseas students. Assistance must be requested when the paper is submitted by choosing this option on the submission website (under "Type"). Further information on travel assistance will be included in the student's author kit. Late News Papers are not eligible for travel assistance or the student paper award.

Pre-Conference Publicity

The accepted 4-page papers and supporting information will be used by IEDM for publicity and portions of these papers may be quoted in pre-conference magazine articles and also via the Web. If this is not acceptable, authors must indicate this on the website when submitting the papers for review. Questions regarding pre-conference publicity should be addressed to the conference public relations managers, Chris Burke at (email: cburke@btbmarketing.com and tel. 1-919-872-8172) and Gary Dagastine (email: gdagastine@nycap.rr.com and tel. 1-518-785-2724).

Agreement Not to Pre-Publish

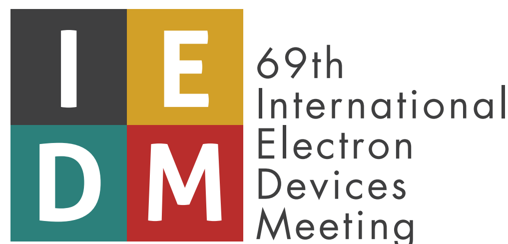
Submission of a paper for review and subsequent acceptance is considered by the committee as an agreement to the IEEE submission policy that the work will not be published by the author prior to the conference. Accepted papers or significant portions of the work must not be published in any other conference presentations with or without proceedings prior to the conference. Violation will be grounds for automatic withdrawal of the paper by the conference committee.

Late News Papers

Deadline for receipt of papers is August 21, 2023.

A very limited number of Late News Papers will be accepted. Late News Papers are not eligible for travel assistance or the student paper award.

Authors are asked to submit late news papers announcing only very recent developments. Papers should be in the same format as a regular paper and should be submitted through the submission web site in the same way as for regular submissions. Authors of accepted papers will be notified by the end of September.



For Further Information

All questions or inquiries for further information regarding this meeting should be directed to the Conference Office at:

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