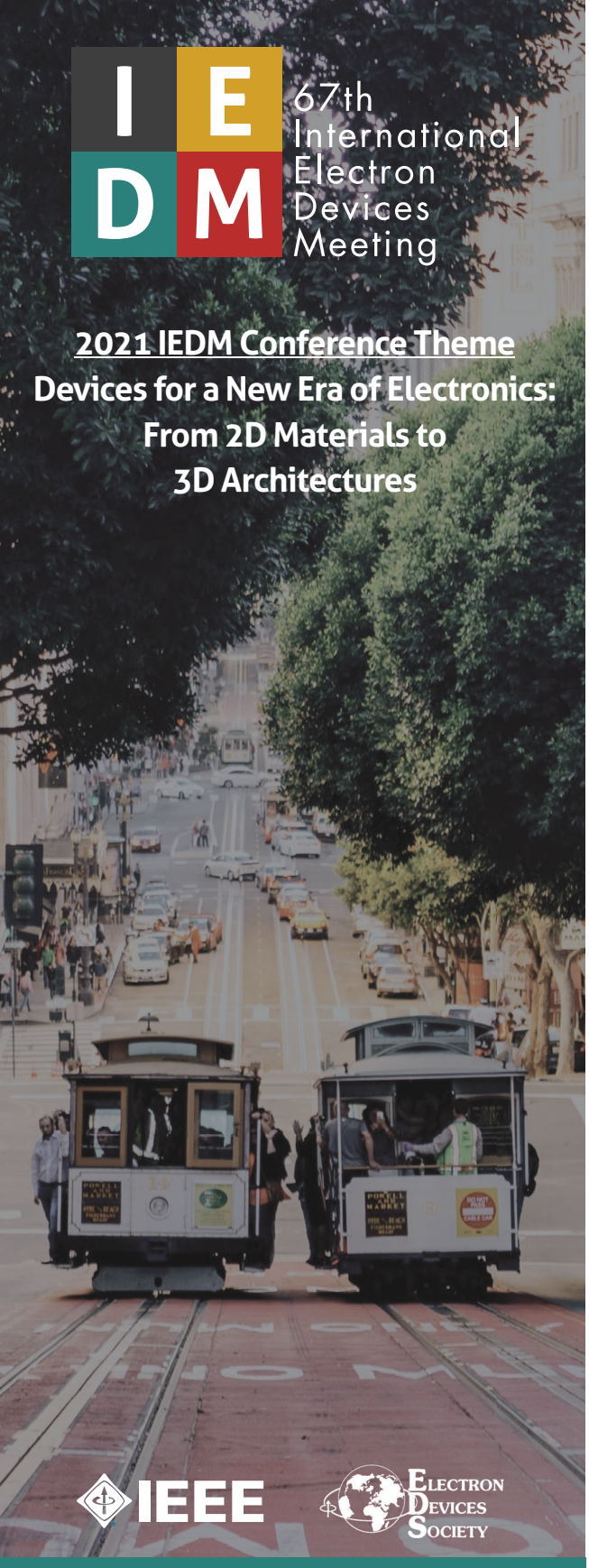

67th International Electron Devices Meeting

2021 IEDM Conference Theme

Devices for a New Era of Electronics: From 2D Materials to 3D Architectures

IEEE

Electron Devices Society

2021 IEEE International Electron Devices Meeting

December 11th – 15th, 2021

Hilton San Francisco Union Square
San Francisco, California

Call for Papers

Submission deadline: July 23rd

Single submission of final, four-page paper

Topics

IEDM encourages submissions in all areas with special emphasis on:

- Neuromorphic computing / AI
- Quantum computing devices
- Devices for RF, 5G, THz and mm-wave
- Advanced memory technologies
- Technologies for advanced logic nodes
- Non-charge-based devices and systems
- Advanced power devices, modules and systems
- Sensors, MEMS and bioelectronics
- Devices/circuits/system interaction
- Package-device level interactions
- Electron device simulation and modeling
- Robustness/security of electronic circuits and systems
- Optoelectronics, displays and imaging systems

Meeting Highlights

- Three plenary presentations by prominent experts
- Special focus sessions covering topics in:
  - Stacking of devices, circuits, chips: design, fabrication, metrology - challenges and opportunities
  - STCO for memory-centric computing and 3D integration
  - Device Technology for Quantum Computing
  - Topological Materials, Devices, and Systems
  - Technologies for AR/VR and intelligent sensors
- Evening panel discussions
- Six tutorial sessions on Saturday, December 11th
- Two short courses on Sunday, December 12th
- Exhibits on December 13th – 15th

For More Information

IEDM Online: ieee-iedm.org

Social Networks:
ieee-iedm.org/social-media

Papers in the Following Areas Are Requested

ADVANCED LOGIC TECHNOLOGY (ALT): Papers are solicited in the areas of CMOS platform technologies and applications (e.g., HPC, LOP, mobile, automotive, low-temperature CMOS, etc.), logic devices and circuits, process integration schemes for advanced nodes, innovations in process module developments, control and metrology techniques, and device technology co-optimization challenges and solutions. Platform technologies include state-of-the-art Si devices, beyond-Si channel materials like Si1-xGex, and advanced transistor architectures such as gate-all-around (stacked) nanowire and nanosheet FETs, extended to the stacking of different polarity devices. Also, of high interest 2.5/3D integration technologies and synergy with CMOS. Topics include devices, interconnects, circuits, novel processes, integration schemes, and scaling approaches/challenges, as well as power-performance-area-cost analysis. Papers addressing process integration of heterogeneous channel materials, substrate and isolation technologies, shallow junctions, scaled gate stacks, channel induced stress and mobility enhancement techniques, contact and via processes, interconnect bottlenecks, sequential and monolithic 3D, heterogeneous chiplets, 2.5/3D integration, advanced packaging, and BEOL compatible transistors are solicited. Process module advancements in EUV lithography, depositions, epitaxy, planarization, etch and self-assembly techniques are also of interest, as well as metrology and process control techniques for reduced defectivity and variability. Submission of papers discussing interactions between advanced technologies, devices/circuits performance and energy consumption, applications-driven hybrid scaling (e.g., CMOS scaling and 2.5/3D integration), tackling of design challenges such as variability, aging, power constraints, physical layout effects, yield implications, carbon footprint, and DTCO solutions are highly encouraged.

EMERGING DEVICE and COMPUTE TECHNOLOGY (EDT): Papers are solicited on emerging nanoelectronic devices and physics. This includes devices based on novel transport and control mechanisms such as tunnel FET, negative capacitance FET, topological materials and devices, phase transitions, ferroelectrics and quantum effects. Devices based on low-dimensional systems including 2D materials, CNTs, nanowires, and quantum dots are welcomed. Neuromorphic compute devices as well as approximate and analog compute and non-charge-based logic such as spintronics are key topics. Furthermore, emerging state machines, continuous time dynamical compute systems are also of interest. Qubit devices as well as devices and systems designed to enable quantum computing, quantum simulation and quantum annealing are of high interest. Papers in EDT focus primarily on device physics, innovative transistor structures, and novel concepts; more mature "platform candidate" papers should be submitted to ALT and MT. Reliability assessment of emerging devices are also solicited here, while assessments for more mature devices should be submitted to RSD.

MEMORY TECHNOLOGY (MT): Papers are solicited in the areas related to embedded and standalone memory technology. This includes advances in both conventional memories including SRAM, DRAM and Flash, and emerging memories including ReRAM, MRAM, PCRAM, FeRAM, crosspoint memory and selectors, organic memory and NEMS-based memory, as well as their applications in the areas of compute-in-memory, and machine learning. Topics span from demonstration of novel device concepts to fully integrated memory arrays, and from product prototyping to manufacturing related challenges and solutions. Demonstrations of manufacturing maturity of emerging memories are of high interest. Submission of papers on novel device concepts and demonstrations, novel integration schemes, novel circuit design schemes, and novel memory architectures that enhance memory performance or improve system level performance in compute-in-memory and AI applications is strongly encouraged.

MICROWAVE, MILLIMETER WAVE and ANALOG TECHNOLOGY (MAT): Papers are solicited in the areas of high frequency device technology, device physics as well as high frequency circuit applications in the micro, mm-wave and THz frequency spectrum. Device physics and technology include based on Si, SiGe, wide bandgap compound semiconductors like III-Vs, III-nitrides, gallium oxide and silicon carbide. Circuit aspects covers analog front ends, filters, beam formers, switches, LNAs, PAs, tunable passives, antenna arrays, SAW/BAW and RF devices for mixed signal, energy harvesting circuit and IoTs, circuit and device interaction for higher system integrity, readout IC targeting quantum computing in the micro and mm-wave domain.

MODELING and SIMULATION (MS): Papers are solicited in the areas of analytical, numerical, and statistical approaches to model electronic and other domain's devices. Topics include physics-based compact and TCAD models for transistors, memories, sensors, and interconnects; modeling and emulation of IC fabrication processes and equipment; atomistic-device multiscale simulation; modeling of interactions between device and circuit/system; modeling of variability, reliability and yield issues; modeling of 3D/heterogeneous integration and advanced packaging. Other beyond-CMOS topics include alternative computing schemes (e.g. neuromorphic and quantum computing), spintronics, ferroelectrics, photonics, and electro-chemical/mechanical device modeling. Submissions should advance the state-of-the-art in modeling and simulation methodology or apply existing techniques to gain new insights into device behaviors.

OPTOELECTRONICS, DISPLAYS, and IMAGING SYSTEMS (ODI): Papers are solicited on optoelectronics, displays, and imaging systems. This includes novel devices, structures, and integration for image sensors, displays, light sources, photonic devices, and high-speed photodetectors and modulators. New technologies on heterogeneous integration of optoelectronics as well as on photonic-electronic integration for optical interconnects, on-chip networks and sensing are welcomed. Papers on quantum photonics and plasmonics for neuromorphic and quantum computation, sensing and encryption are also of interest. Furthermore, ODI includes CMOS imagers, high-speed and high-time resolution imagers, CCDs, stacked image sensors, and displays of all types. In addition, papers on displays for augmented or virtual reality, holography, TFTs for photonics applications, flexible, stretchable, and/or printed electronics, in-display sensors are encouraged. Papers on displays or light emitting devices with novel materials such as perovskites or quantum dots are also of interest. We particularly welcome submissions concerning optoelectronic or photonic devices or systems based on topological concepts.

POWER DEVICES and SYSTEMS (PDS): Papers are solicited on discrete and integrated power devices, modules and systems using Si, diamond, and compound semiconductors. Papers exploring the system-level impact of power devices are also of interest. Topics of interest include power devices (diodes, BJTs, FETs, superjunction devices, IGBTs, HEMTs, etc.), and materials (Si, Diamond, SiC, GaAs, GaN, AlN, Ga2O3, etc.), manufacturing processes, device design, modeling (TCAD and compact models), physics, and reliability. Devices targeting the full range of power and power conversion applications, including automotive, power supplies for computers and data centers, power conditioners for photovoltaic, motor drives and smart grid (solid-state transformers and HVDC transmission), and wireless power transfer, are of interest besides fundamental studies on doping, deep-level traps, interface state densities and device reliability for power switching devices

RELIABILITY OF SYSTEMS and DEVICES (RSD): Papers are solicited in all areas of electrical and physical characterization, reliability evaluation and yield analysis of transistors, interconnects, circuits and systems mainly (but not limited) to Si-based technologies. Specific reliability topics include, for FEOL: transistor degradation due to hot carriers and bias temperature instabilities; dielectric wear-out and breakdown; self-heating effects; process charging damage; latch-up and ESD; soft error mechanisms in logic and memories. For MEOL/BEOL topics include: electromigration failure of contacts and interconnects; breakdown of BEOL dielectrics and MEOL spacers; thermal management; For system and circuit reliability topics include design for reliability and variability-aware design, robustness and security of electronic circuits and systems. Of particular interest are investigations of degradation mechanisms for devices, circuits and systems in the following area: emerging memories; more-than-Moore applications; biomedical devices and systems; automotive and aerospace

SENSORS, MEMS, and BIOELECTRONICS (SMB): Papers are solicited in the areas of sensors, micro/nano electromechanical systems (MEMS and NEMS), microfluidics and BioMEMS, with particular emphasis on new device concepts, integrated implementations, CMOS-on-MEMS, embedded intelligence, organic-inorganic hybrid microfabrication, flexible devices, and multi-sensors on a chip for wearable and IoT applications. Sensors includes chemical, molecular and biological detection based on acoustic, electrical, electrochemical, magnetic, mechanical and optical principles. Topics of interest in the MEMS area include actuators, physical sensors, resonators, integrated inertial measurement units, TFTs, RF MEMS, micro-optical and optomechanical devices, micro-power generators, and devices for energy harvesting as well as on-chip energy storage. BioMEMS area covers organic-inorganic hybrid devices, point-of-care biomedical devices, bio-electronic interface, integrated biomedical sensing and implantable neural interfaces.

Preparation of Full Papers

Papers must be submitted electronically in IEEE Xplore-compatible pdf format. The deadline for submission of papers is July 23rd, 2021. PRIOR to preparing your paper for electronic submission, please read the paper preparation and submission guidelines below. A paper template and sample paper are available at: ieee-iedm.org/preparation-of-papers.

Papers Must Clearly State

- The purpose of the work
- The manner and degree to which it advances the art accompanied by proper references
- Specific new results that have been obtained with clear experimental conditions and their significance

The degree to which the paper deals with these issues will strongly affect whether the paper is accepted. The most common cause of rejection of submitted papers is a lack of specific results. Only work that has not been previously published nor submitted elsewhere at the time of the conference will be considered. Paper acceptance will be based solely on the information provided on the four page paper submitted. Promises of upcoming results will be ignored. All submissions will be checked for plagiarism.

Electronic Submission

Only electronic submissions through the paper submission system linked to the conference website will be accepted. Do not email files to the conference office. In order for your paper to receive a full review, the following information MUST be entered on the website along with your submission:

- Title of paper
- Name, complete mailing address and phone, and email of first author
- Names, affiliations, city, state, country of additional authors
- Person to whom correspondence should be sent, if other than the first author
- Identification as invited or student paper and student travel request, if applicable
- Suggested area (as listed in this announcement) into which the paper fits
- 50-word abstract

Papers Must Include

- Title of paper
- Name, complete mailing address, phone, and email of first author and name, affiliation, city, state and country of additional authors
- Up to two pages of text and up to two additional pages of figures and drawings (no text, captions only) in 8-1/2" x 11" format describing the planned 20-minute paper and emphasizing the findings. The font size for the body of the text and in figures and captions must be at least 10 point.
- Excessive photo reduction of figures and poor legibility will negatively impact acceptance
- Papers with more than 2 pages of text or figures shall be grounds for immediate rejection
- Please avoid the use of special international fonts

50-Word Web Page Abstract

This abstract is a brief synopsis (50 words) of your paper. Accepted 50-word abstracts will be used in preparing the IEDM web pages. The abstract should be prepared and provided during the submission process in the requested text field on the submission web site. DO NOT INCLUDE the 50-word abstract as a separate page with your submission.

For questions contact the conference office:
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Notification of Acceptance

Authors of accepted papers will be notified by the end of September. The accepted paper will be published as-is in the Technical Digest of the 2021 IEDM. Publication in the digest in no way precludes later publication of a fuller account of the work in another journal, but NO PUBLICATION is acceptable before the conference. The paper must be presented at the conference by one of the listed authors.

Student Presentation of Papers Encouraged

Papers presented by students and based on their own work will be considered for the Best Student Paper Award. The paper must be identified as a student paper at the time of submission. The award is based on both the paper and the presentation which must be given by the student. The award will be announced and presented at the 2021 IEDM.

Student Speaker Financial and Travel Assistance

Financial assistance for travel and registration is available to students presenting papers. This applies also for overseas students. Assistance must be requested when the paper is submitted by choosing this option on the submission website (under "Type"). Further information on travel assistance will be included in the student's author kit. Late News Papers are not eligible for travel assistance or the student paper award.

Pre-Conference Publicity

The accepted 4-page papers and supporting information will be used by IEDM for publicity and portions of these papers may be quoted in pre-conference magazine articles and also via the Web. If this is not acceptable, authors must indicate this on the web site when submitting the papers for review. Questions regarding pre-conference publicity should be addressed to the conference public relations manager, Chris Burke at (email: cburke@btbmarketing.com and tel. 1-919-872-8172) and Gary Dagastine (email: gdagastine@nycap.rr.com and tel. 1-518-785-2724).

Agreement Not to Pre-Publish

Submission of a paper for review and subsequent acceptance is considered by the committee as an agreement to the IEEE submission policy that the work will not be published by the author prior to the conference. Accepted papers or significant portions of the work must not be published in any other conference presentations with or without proceedings prior to the conference. Violation will be grounds for automatic withdrawal of the paper by the conference committee.

Late News Papers

Deadline for receipt of papers is August 30, 2021.

A very limited number of Late News Papers will be accepted. Late News Papers are not eligible for travel assistance or the student paper award.

Authors are asked to submit late news papers announcing only very recent developments. Papers should be in the same format as a regular paper and should be submitted through the submission web site in the same way as for regular submissions. Authors of accepted papers will be notified by the end of September.

IEDM 67th International Electron Devices Meeting

For Further Information

All questions or inquiries for further information regarding this meeting should be directed to the Conference Office at:

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