CALL FOR ABSTRACTS

ASMC

Advanced Semiconductor Manufacturing Conference—ASMC 2021

With technical support from

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SEMI and IEEE invite authors to submit a technical abstract to ASMC 2021. ASMC is the leading international technical conference for exploring solutions to improve the collective microelectronics manufacturing expertise. Solving the challenges presented by semiconductor manufacturing is an ongoing collaborative effort by customers, device makers, equipment and materials suppliers, and academia. The conference provides an unparalleled platform for semiconductor professionals to network and learn the latest information in the practical application of advanced manufacturing strategies and methodologies.

CALL FOR ABSTRACTS—SUBMIT HERE

ASMC is now soliciting abstracts from professionals involved in all areas of semiconductor manufacturing. Authors of selected papers will have an opportunity to present their work at the conference. They also may receive an invitation to publish their paper in a special section of ASMC 2021, which will be featured in IEEE Transactions on Semiconductor Manufacturing. ASMC 2021 could be held as a virtual event depending on progress in containing COVID-19. Whether the event is on-site or virtual, all technical papers accepted for presentation will be published by IEEE. If the conference takes place in person, speakers would be given the option to present live or virtually. If held online, all speakers would be expected to deliver their presentations virtually.

AWARDS

- **ASMC 2021 ENTEGRIS BEST PAPER AWARD**
  All papers presented at ASMC will be considered for the ASMC 2021 Entegris Best Paper Award.

- **ASMC 2021 GLOBALFOUNDRIES BEST STUDENT PAPER AWARD**
  Papers authored and presented by a student or student/professor will receive special consideration for the 2021 ASMC Outstanding Student Paper competition, sponsored by GLOBALFOUNDRIES. Please indicate in the abstract if the paper will be authored by a student.

LOCATION

Saratoga Springs
New York, USA

QUESTIONS

Paul Cohen
pcohen@semi.org

For templates and further instructions, visit:
www.semi.org/asmc

IMPORTANT DATES (subject to change)

Abstracts Due:	October 30, 2020
Author Notification:	December 15, 2020
Manuscripts Due:	February 9, 2021
Final Manuscripts Due:	April 6, 2021
Presentations Due:	April 20, 2021
Conference Dates:	May 3-6, 2021

AUTHOR INSTRUCTIONS

Original, non-commercial, non-published works are being solicited in specific categories. Peer-reviewed papers are selected based on a clear outline of the problem, analysis, solution/results and conclusions. Papers co-authored between customers, device manufacturers, equipment or materials suppliers, and/or academic institutions (including students) that demonstrate innovative, practical solutions for advancing semiconductor manufacturing are highly encouraged. Authors should:

- Provide an extended abstract of no more than two pages (max. of 1000 words, MS Word or PDF) with supporting data, charts, figures embedded in the last page.

- Summarize the topic and theme in as much detail as allowed by the word count limitation. Include title, author(s), company affiliation(s), contact information, topic and five key words describing the work.

- The final paper, in the ASMC template found in Author Kit must show a complete set of data to support initial abstract.

Peer-reviewed papers are selected based on a clear outline of the problem, analysis, solution/results and conclusions. Authors who prefer to present in the poster session must indicate this request on their abstract.

ASMC 2021 Call for Paper Topics

AM: Advanced Metrology
Development of new metrology techniques and methodologies; *in-situ* monitoring methods; metrology for process control; measuring critical dimensions, overlay, films; metrology of next-generation materials, processes and architectures (TSV, FinFETs, EUV, etc.); scatterometry with reflectometry or ellipsometry; pros and cons of machine learning in measurement signal analysis wide-bandgap semiconductors; novel extension of existing metrology tools as well as evaluation of upcoming measurement technologies to meet HVM requirements.

AEPM: Advanced Equipment Processes and Materials
Development of new front- and back-end processes; characterization and integration of barrier layers, advanced gates, high-κ and low-κ, isolators, optical and conducting materials; evaluation of novel substrates; methodologies for driving new materials from R&D to mass production.

AP/DFM: Advanced Patterning / Design for Manufacturability
Immersion, double/multiple patterning, and EUV lithography; advanced resolution enhancement techniques; source/mask optimization; alignment and overlay enhancement solutions; edge placement error measurement; advanced reticles; alternative patterning methods; directed self-assembly; feedforward control solutions; high versus low volume manufacturing effects on lithography processes; computational lithography; process models and process model files; optical proximity correction and verification; design rule creation and verification; DFM in support of yield learning through product cycle; early manufacturing involvement; integrated product and process development (IPPD).

APC: Advanced Process Control
Advanced control techniques such as run-to-run control; model-based control; non-linear control methods; application of advanced statistical methods to control; advanced SPC techniques; fault detection and classification (FDC); virtual metrology.

CFM: Contamination Free Manufacturing
Backside contamination, ultraclean technologies, materials, control of mini-environments, FOUP cleanliness and control, vibration monitoring, vibration control, wafer and reticle carriers/transport, ESD control, EUV lithography.

DM: Big Data Management and Mining
Fab and test floor data collection methods and analysis; data format, volume and interface challenges; fast drill-down to problem tools and sources; foundry-to-fabless data transfers and information issues; new visualization methods for improved data understanding; applying data mining techniques and machine learning based approaches to isolate and utilize critical information from large data volumes; data ownership.

DI: Defect Inspection and Reduction
New brightfield, darkfield, e-beam and other techniques and technologies for cost-effective yield control; process development using defect detection and management; new methodologies for detection, characterization, classification and disposition of defect counts, types and distributions; diagnostic techniques to correlate in-line inspection results to product yield and defectivity.

DP: Discrete and Power Devices
Solutions manufacturers facing challenges other than smallest feature sizes, including analog/mixed-signal applications for automotive devices, power management and display drivers.

EO: Equipment Optimization
Efficiency/productivity measurements; optimizing and extending fab productivity within the framework of existing wafer sizes; cycle time reduction; cost reduction; best practices; customer-supplier continuous improvement programs; CMP Development; high mix/high-volume factories with high-equipment productivity; small-lot manufacturing and single-wafer/mini batch tools; fab conversions; integration of factory control systems into complete supply chain.

FA: Factory Automation
Automation in fab; probe; assembly and test factories; e-diagnostics; e-manufacturing; WIP management; scheduling; planning; logistics; modeling; productivity; supply chain management; manufacturing performance; capacity, metrics, supply/demand management; deployment, cycle time and time-to-market; fully automated factory and remote operation center equipment and equipment interfaces; data collection interfaces; automated material handling systems (AMHS) challenges and carriers; standards and standardization.

FE: The Fabless Experience
Challenges faced by fabless semiconductor companies; integrating material from multiple sources; strategies for managing risk due to supply shortages and out of spec. parts; foundry strategies for effectively supplying many customers; foundry methods for controlling costs for small orders; related topics of general interest to fabless semiconductor companies or foundries.

GF: Green Factory
The role of environment; health and safety; emissions and effluents control; energy saving; recycling; safety and health; community involvement; ergonomics; zero emission; global environment protection; waste reduction; sustainability.

IE: Industrial Engineering
Facilities design and layout; equipment design and AMHS interactions; manufacturing systems design; statistics/quality; computer modeling; simulation; systems management; human factors in engineering; financial decision making; cost reduction; supply chain.

ISD: Innovative Silicon Devices and Processes
MEMS, PCM, silicon photonics, magnetic heads, micro displays, sensors, DLP, MRAM, organic semiconductor, silicon modulators, novel structures, carbon nanotube, graphene, interconnects; novel and emerging applications of existing process techniques.

LM: Lean Manufacturing
Establishing flow; standards and standard work; value stream mapping; Kaizen; Kaikaku; cycle times; WIP; 5S; continuous improvement; metrics, training within industry (TWI); waste reduction.

NS/NC: Non-silicon and Non-CMOS
SiC, GaN, GaAs, glass and quartz wafers, heterogenous devices, sub 200-mm manufacturing, analog/mixed signals, power devices, automotive, power management, flexible substrates, display drivers

SM: Smart Manufacturing
Smart manufacturing systems, equipment and technologies; supply chain modeling and networks; system integration for manufacturing integration; crowdsourcing design for manufacturing; manufacturing process simulation and optimization; information technology; smart and intelligent manufacturing processes; cloud-enabled manufacturing systems and applications; industrial Internet of Things; next-generation robotics/automation; measurement and systems monitoring; business, health & safety, processes, and cost learnings.

YE: Yield Enhancement/Learning
Yield analysis tools and methods, including identifying root cause of yield loss and reliability fails; failure analysis; defect-to-yield correlation; zonal and spatial pattern analysis; slot signature analysis; use of volume diagnostics for pinpointing net failures; determination of critical particle size and types.

YM: Yield Methodologies
Yield monitoring and modeling accuracy; model types; critical area extraction techniques; yield-targeted data mining; modeling of systematic and parametric yield; process sector analysis; short-flow yield programs.

3D/TSV: Packaging and Through Silicon Via
3D integration in general and associated topics like wire bonding, flip chip bonding (bump metallization), micro-bump bonding, C4 New Process, through wafer vias, silicon carrier; Novel approaches to global/local interconnect issues, power delivery and thermal management.