

54th IEEE Semiconductor Interface Specialists Conference

December 13–16, 2023 (Tutorial: December 13) Bahia Resort Hotel, San Diego, CA www.ieeesisc.org



Executive Committee

P. D. Ye, General Chair Purdue U., USA

J. Rozen, Program Chair IBM, USA

J. Franco, Arrangements Chair imec, Belgium

W. Vandenberghe, *Ex-Officio* UT Dallas, USA

Program Committee

D. Chen ASU, USA

J. Coignus CEA/LETI, France

C. L. Hinkle Notre Dame U., USA

D. Jena Cornell U., USA

A. Khan Georgia Tech, USA

E. Lind Lund U., Sweden

C. Liu National Taiwan U., Taiwan

S. Migita AIST, Japan

M. Passlack TSMC, USA

R. Pillarisetty Intel, USA

J. Robertson Cambridge U., UK

T. Roy, Duke U., USA

R. Timm Lund U., Sweden

W. Tsai Stanford U., USA

Y. Wu PKU, China

G. Xiao National U. of Singapore, Singapore

C. Yang Applied Materials, USA



Call for Papers

The SISC is a workshop-style conference that provides a forum for device engineers, solid state physicists, and material scientists to discuss topics of common interest, formally through invited and contributed presentations, and informally during poster and rump sessions. SISC is sponsored by the IEEE Electron Devices Society and is held right after IEDM.



This year, SISC will be held as a fully in-person event.

The program includes talks and poster presentations (*theory and experiment*) on the role of materials and their interfaces on performance and reliability of:

- Logic Devices for future technology nodes (Nanosheet, CFET, VFET, etc.),
- Insulators on High-Mobility substrates (SiGe, Ge, etc.),
 - Non-Volatile Memory for AI / In-Memory / Neuromorphic Compute (ReRAM, PCM, ECRAM, etc.),
- Wide Bandgap semiconductor power devices (SiC, GaN, β-Ga₂O₃, etc.),
- Ferroelectric devices (FET, memory, etc.),
- Steep Sub-Threshold slope logic devices (Tunnel FETs, etc.),
- 2D materials and devices,

٠

Monolithic and/or Heterogeneous ICs (BEOL oxide transistors, interconnects, packaging, etc.),

including machine learning / materials discovery techniques developed and used for their study.

Confirmed Invited speakers

- Prof. Masaharu Kobayashi, U. Tokyo, Japan Oxide Semiconductor Transistors for LSI Application
- Dr. Anabela Veloso, imec, Belgium Entering a New Era of Nanosheet-based FET Device Architectures with Increased FEOL-BEOL Synergies Prof. Sarit Dhar, Auburn University, USA
- Interface Trapping and Scattering in 4H-SiC MOSFETs
- **Prof. Daniel Gall**, RPI, USA Interconnects: New Materials for High Conductivity
- **Dr. Ashish Penumatcha**, Intel, USA Enabling Gate-Pitch Scaling in the Angstrom Era
- Prof. Bilge Yildiz, MIT, USA Protonic Electrochemical Synapses for Analog Deep Learning and Beyond
 Prof. Enxia Zhang, Vanderbilt University, USA
 - Radiation Effects and Reliability of 3D ICs

Wednesday evening Tutorial

• **Dr. Dale McHerron**, IBM, USA From Interconnects to Chiplets: Materials and Interfaces for Advanced Packaging

A Best Student Presentation Award will be given in memory of E. H. Nicollian.

A Best Poster Award will be given in memory of T. P. Ma.

Abstract submission deadline: August 6, 2023

Abstract submission, previous technical programs, contact information, etc.: <u>https://www.ieeesisc.org</u>